REMARKS

Claims 1, 20, 32, and 35 have been amended. Claim 14 has been canceled. New claims 55 and 56 have been added. Claims 1-13, 15-37, and 55-56 remain pending. The specification has been amended to correct certain informalities. Figure 5C has been amended as stated in the Amendments to the Drawings. Applicant respectfully requests reconsideration of the rejections in light of this reply.

Claims 1-4, 11, 14-20, and 28-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,117,702 ("Nakamura") in view of U.S. Patent No. 6,232,626 ("Rhodes"). This rejection is respectfully traversed.

Claim 1 recites, *inter alia*, a pixel cell comprising a photodiode, "the photodiode being formed within a substrate and below an upper surface thereof and comprising at least two of a first layer having a first band gap and at least two of a second layer having a second band gap, wherein the first layers are alternated with the second layers; a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode; and a graded buffer layer beneath a bottom layer of the photodiode."

Applicant respectfully submits that the subject matter defined in claims 1 and 20 is not taught or suggested by the cited combination of references. The graded buffer layer reduces strain from lattice mismatch by changing the composition of the graded buffer layer from a bottom portion to a top portion such that the composition of the bottom portion of the graded buffer layer approximately equals the composition of the substrate and the composition of the top portion of the graded buffer layer approximately equals the composition of the bottom layer of the photodiode. *See* Specification at 13, ¶ [0059].

Nakamura and Rhodes even when combined together do not disclose, teach or suggest the claimed subject matter. The Office Action points to FIG. 5 of Nakamura as teaching the claimed photodiode. However, the FIG. 5 photosensitive structure of Nakamura is not part of a pixel cell and is not "formed within a substrate and below an upper surface thereof," as recited in claim 1. Nakamura's photosensitive structure (FIG. 5) is a laminated structure, but is not disclosed as being formed within a substrate and below an upper surface thereof and is not disclosed as being part of a pixel cell. Nakamura also fails to disclose "a gate of a transistor

adjacent to the photodiode for transferring the amplified charge from the photodiode," as recited in claim 1. Rhodes discloses a pixel cell with a trench photosensor, but also fails to disclose the claimed photodiode. Moreover, there is no reason evident in Nakamura or Rhodes for one skilled in the art to combine the references and form a pixel cell comprising "a photodiode for generating charge in response to light and for amplifying the generated charge, the photodiode being formed within a substrate and below an upper surface thereof and comprising at least two of a first layer having a first band gap and at least two of a second layer having a second band gap, wherein the first layers are alternated with the second layers; [and] a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode," as recited in claim 1.

Moreover, Nakamura does not teach or suggest the claimed graded buffer layer below the photodiode. Rather, Nakamura states that layer 23 (FIG. 5) is "an electron-injection inhibition layer" which is "formed by [depositing] a p^+a—Si layer" and that layer 24 (FIG. 5) is "an optical absorption layer . . . made of a semiconductor layer obtained by depositing a—Si." Nakamura at col. 14, ll. 45-55. Rhodes too fails to disclose a graded buffer layer below the disclosed trench photodiode.

For at least these reasons, the cited combination of references fails to teach or suggest a "photodiode for generating charge in response to light and for amplifying the generated charge, the photodiode being formed within a substrate and below an upper surface thereof and comprising at least two of a first layer having a first band gap and at least two of a second layer having a second band gap, wherein the first layers are alternated with the second layers; [and] a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode," as recited in claim 1.

Claim 20 recites, *inter alia*, an image sensor comprising "an array of pixel cells at a surface of a substrate, wherein at least one of the pixel cells comprises a photodiode formed within the substrate and below an upper surface thereof, the photodiode comprising at least two of a first layer comprising a first material and at least two of a second layer comprising a second material, . . . wherein the first layers are alternated with the second layers; a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode; and a

graded buffer layer beneath a bottom layer of the photodiode." Applicants respectfully submit that the cited references fail to teach or suggest these elements of claim 20 for similar reasons as set forth above with respect to claim 1.

Claims 2-4, 11, and 15-19 depend from claim 1 and are allowable along with claim 1. Claims 28-31 depend from claim 20 and are allowable along with claim 20. Accordingly, Applicant respectfully requests the withdrawal of the rejection and allowance of the claims.

Claims 5-10, 12-13, 21-27, and 32-37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura in view of Rhodes in view of U.S. Patent No. 5,818,322 ("Tasumi"). This rejection is respectfully traversed.

Applicant respectfully submits that the cited combination of references fails to teach or suggest a photodiode "formed within [a] substrate and below an upper surface thereof," "a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode; and a graded buffer layer beneath a bottom layer of the photodiode," as recited in claim 1. The cited combination of references also fails to teach or suggest a photodiode "formed below an upper surface of a substrate," "a gate adjacent to the photodiode for transferring the amplified charge from the photodiode; and a graded buffer layer formed within the substrate and below the photodiode," as recited in claim 32. With respect to claim 35, the cited combination does not teach or suggest a photodiode "formed below an upper surface of a substrate," "a graded buffer layer formed beneath the photodiode; a gate of a transistor adjacent to the photodiode; a floating diffusion region electrically connected to the first transistor; and readout circuit electrically connected to the floating diffusion region." Although claims 1, 20, 32, and 35 are different in scope, the arguments set forth above with respect to Nakamura and Rhodes hold true for claims 32 and 35.

Tasumi, which has been cited as teaching a photodiode structure with Si and SiGe formed in the groove of the photodiode (*see* Office Action at 5), fails to cure the deficiencies of Nakamura and Rhodes set forth above. Tasumi does not disclose a graded buffer layer. Accordingly claims 1, 20, 32, and 35 are patentable over the cited combination of references.

Moreover, Applicant respectfully submits that the cited combination of references fails to teach or suggest a photodiode wherein "[a] first layer is Si_xGe_{1-x} and [a] second layer is Si_yGe_{1-y}," as recited in claim 9 and wherein "[a] first material is Si_xGe_{1-x} and [a] second material is Si_yGe_{1-y}," as recited in claim 25. The cited combination also fails to teach or suggest a photodiode wherein "[a] first layer is $Si_xGe_{1-x}C_z$ and [a] second layer is $Si_xGe_yC_z$," as recited in claim 10 and wherein "[a] first material is $Si_xGe_{1-x}C_z$ and [a] second material is $Si_xGe_yC_z$," as recited in claim 26. Contrary to the assertions set forth in the Office Action, none of the cited references specifically teach or suggest the claimed compositions for the photodiode layers. Accordingly, claims 9, 10, 25, and 26 are patentable over the cited combination of references.

In addition, the cited combination fails to teach or suggest that layers of a photodiode are formed of materials "selected from the group consisting of Si, Si_xGe_{1-x}, $Si_xGe_{1-x}C_y$, GaAs, GaAlAs, InP, InGaAs, and InGaAsP," as recited in claims 5, 21, and 35. The cited references do not teach or suggest all of the claimed compositions, namely, forming photodiode layers using GaAlAs, InP, InGaAs, or InGaAsP. Accordingly, claims 5, 21, and 35 are patentable over the cited combination of references.

For at least these reasons, claims 1, 5, 9, 10, 20, 21, 25, 26, 32, and 35 are patentable over the cited combination. Since claims 5-10, 12-13, 21-27, 33, 34, 36, and 37 depend from an allowable base claim, they are also patentable. Accordingly, Applicant respectfully requests the withdrawal of the rejection and allowance of the claims.

Newly added claim 55 recites a "photodiode for generating charge in response to light and for amplifying the generated charge, the photodiode being formed within a substrate and below an upper surface thereof and comprising at least two of a first layer having a first band gap and at least two of a second layer having a second band gap, wherein the first layers are alternated with the second layers; and a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode." Claim 55 is patentable over Nakamura, Rhodes, and Tasumi for similar reasons set forth above with respect to claim 1. Specifically, the references do not teach or suggest the photodiode of claim 55 "being formed within a substrate and below an upper surface thereof," and a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode.

Newly added claim 56 recites a "a photodiode for generating charge in response to light and for amplifying the generated charge, the photodiode comprising at least two of a first layer having a first band gap and at least two of a second layer having a second band gap, wherein the first layers are alternated with the second layers; a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode; and a graded buffer layer beneath a bottom layer of the photodiode." Claim 56 is patentable over Nakamura, Rhodes, and Tasumi for similar reasons set forth above with respect to claim 1. Specifically, the references do not teach or suggest an image sensor comprising the photodiode of claim 56, "a gate of a transistor adjacent to the photodiode for transferring the amplified charge from the photodiode; and a graded buffer layer beneath a bottom layer of the photodiode."

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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